MULTIMEDIA ◖●◗ UNIVERSITY

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FINAL EXAMINATION

TRIMESTER 3, 2017/2018

ENT3036 – SEMICONDUCTOR DEVICES
(NE)

6 JUNE 2018
2.30 p.m. - 4.30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages with 4 Questions only.

2. Attempt All questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Useful constants and coefficients:

Physical Constants

Boltzmann's constant (k)	1.3807×10^{-23} JK^{-1}
	8.617×10^{-5} eVK^{-1}
Planck's constant (h)	6.626×10^{-34} Js
Thermal voltage@300K kT/e	0.0259 V
kT	0.0259 eV
Electron mass in free space (m_e)	9.10939×10^{-31} kg
Electron charge (e)	1.60218×10^{-19} C
Permeability of free space (μ_0)	$4\pi \times 10^{-7}$ Hm^{-1}
Permittivity of free space of free space (ε_0)	8.85×10^{-12} Fm^{-1}
Avogadro's number (N_A)	6.022×10^{23} atoms/mol

Question 1

(a) Consider a silicon PN junction at thermal equilibrium condition without external bias at $T = 300$ K has dopant concentrations of $N_a = 2 \times 10^{17} cm^{-3}$ on the P-side and $N_d = 8 \times 10^{15} cm^{-3}$ on the N-side. Given that intrinsic carrier density, $n_i = 1.5 \times 10^{10} cm^{-3}$.

(i) Calculate the Fermi level on each side of the junction with respect to the intrinsic Fermi level.

[4 marks]

(ii) Sketch the energy band diagram for the PN junction at equilibrium condition. Draw the Fermi level throughout the junction in relation to the conduction and valence band edge and briefly explain your diagram.

[4 marks]

(iii) Determine the height of potential barrier at the junction in your energy band diagram of part (a)(ii) and the internal built-in potential voltage, V_{bi}.

[4 marks]

(iv) With the aid of energy band diagrams, explain the current conduction processes in the PN junction under forward- and reverse-biased conditions in relation to the potential barrier height.

[6 marks]

(b) Figure 1(b) shows the cross section of an NPN transistor with the lateral distribution of base current. The emitter current crowding effect is one of the non-ideal effects that could occur in the bipolar junction transistor with base region less than a micrometer thick, causing the bipolar junction transistor to deviate from its ideal characteristics.
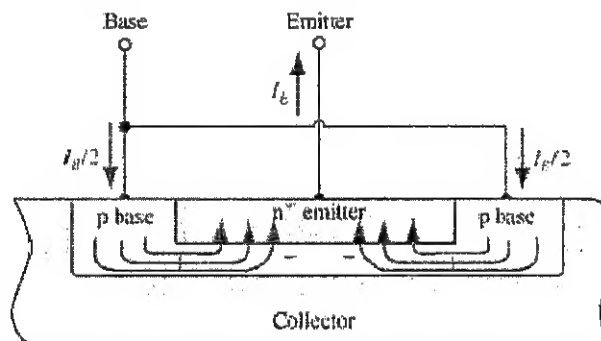

Figure 1(b)

(i) Explain the current crowding effect in a bipolar junction transistor and relate how it affects the performance of the transistor.

[3 + 2 marks]

(ii) Suggest two methods to minimise the current crowding effect.   [2 marks]

Continued....

Question 2

(a) Figure Q2(a) shows $I_D - V_{DS}$ characteristic curves of a symmetrical n-channel JFET for $V_G = 0\,\text{V}$ and $V_G < 0\,\text{V}$. With the aid of simple diagrams for gate-to-channel space charge region, explain the operation principle of this n-channel JFET and how the drain current in an n-channel JFET is reduced as the gate voltage is made more negative.
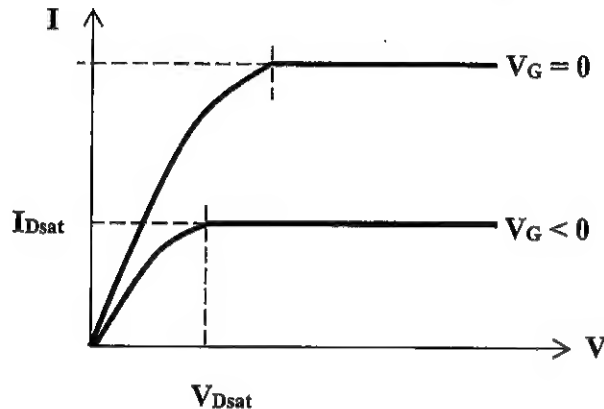
[11 marks]

Figure Q2(a)

(b) Consider a p-channel MOSFET with a polysilicon gate has a substrate doping density of 5×10^{22} donors/m³. The oxide is 10^{-7} m thick and has 10^{15} oxide surface charges/m². The transistor is operating at room temperature and assume that $\Phi_{ms} = 0$.

   (i) Assuming that the source is connected to the substrate, deduce the required operating polarities of the gate-source and drain-source voltages.

[2 marks]

   (ii) Calculate the threshold voltage and explain why the device is in enhancement mode.

[8 marks]

   (iii)Find the minimum surface doping density and type of dopant required to make the MOSFET a depletion mode device.

[4 marks]

Continued....

Question 3

(a) Consider an ideal MOS structure with p-type semiconductor substrate doped to $N_a = 3 \times 10^{15} cm^{-3}$, a silicon dioxide insulator with a thickness of $t_{ox} = 40\,nm$, and an aluminum gate. Assume that the area of the gate is a 100 μm² and T = 300 K.

    (i) Sketch the general shape of the high-frequency C-V characteristic for this capacitor.

                                                                             [2 marks]

    (ii) Calculate the capacitance of the insulator, C_i.   [2 marks]

    (iii) If $V_G = V_T$, determine the surface potential ϕ_s.   [2 marks]

    (iv) Evaluate the minimum capacitance value of the MOS system.   [5 marks]

    (v) Evaluate the threshold voltage V_T.   [3 marks]

    (vi) Sketch another C-V characteristic on the same axes, indicating all the qualitative changes that occur if the substrate doping is increased.   [2 marks]

(b) (i) Derive the expressions for the saturated drain current, I_D, and the transconductance, g_m, of a MOSFET, taking as a starting point the drain current characteristic equation:

$$I_D = \frac{W\mu C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2 \right]$$

    where the symbols have their usual meaning.   [4 marks]

    (ii) At $V_D = 1.5V$ and $V_G = 4.0V$ the MOSFET with threshold voltage $V_T = 1.0V$ exhibits a drain current of $3.5 \times 10^{-4} A$. Determine the I_D if $V_G = 4.0V$ and $V_D = 4V$.   [5 marks]

Continued....

Question 4

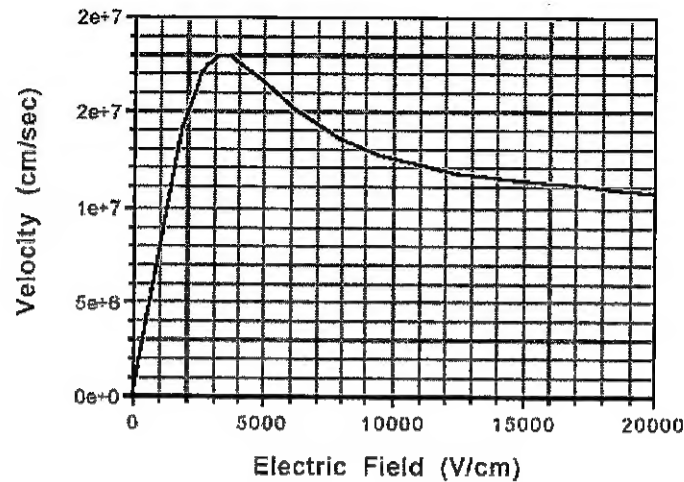(a) Figure Q4 shows the electron drift velocity of GaAs as a function of applied electric field at 300 K.

Figure Q4

(i) For electric fields above $E_c = 3 \times 10^3 \, V/cm$, the electron drift velocity decreases with increasing electric field, leading to a negative differential resistance. With the aid of a simple band diagram, explain this phenomenon.

[7 marks]

(ii) Sketch the electric field and carrier density as a function of position in a GaAs Gunn diode and describe how a domain is formed.   [8 marks]

(iii) For a Gunn diode operating in the "transit time" mode, how are the frequency, length L of the device, and drift velocity v related?

[3 marks]

(iv) For a 10 GHz oscillation frequency, approximately how long should a Gunn diode be if it is made out of GaAs? Assume the domain will drift across the diode with $v = 10^7 \, cm/s$.

[3 marks]

(b) What are the effects that cause the IMPATT diodes exhibit a differential negative resistance?

[4 marks]

End of the paper